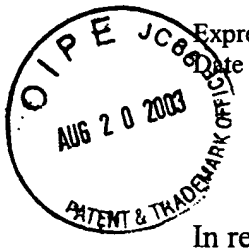
Rev. 08/01/2003

08-22-03 AF/2700

Attorney Docket No.: NVID-018/00US **PATENT**
Client Reference No.: P000177



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Date of Deposit: **August 20, 2003**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of James M. VAN DYKE, et al.

Serial No.: 09/687,453 Examiner: Chen, Chongshan

Confirmation No.: 1345 Art Unit: 2172

Filed: October 13, 2000

For: **CONTROLLER FOR A MEMORY SYSTEM HAVING MULTIPLE PARTITIONS**

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF RESPONSE

Enclosed are the following documents in response to the Final Official Action dated June 20, 2003, for the above-identified application:

[X] Amendment/Response
[X] Return receipt postcard

The fee has been calculated as follows:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEE
Total Claims	**36**	- 36 =	**0**	x $18.00	$0.00
Independent Claims	**2**	- 3 =	**0**	x $84.00	$0.00
If multiple dependent claims are presented, add $280.00					
Total Amendment Fee					
If small entity status is applicable, subtract 50% of Total Amendment Fee					
Other fees: (specify)					
TOTAL FEE DUE					$0.00

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 03-3117.

Dated: Aug. 20 2003

Respectfully submitted,
COOLEY GODWARD LLP

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RESPONSE

This communication is responsive to the final rejection mailed June 20, 2003. Reconsideration of the rejected claims is respectfully solicited in view of the following comments.

All of the claims are rejected in view of Kurihara (U.S. Patent 5,500,939). With respect to independent claim 32, the examiner acknowledges, "Kurihara does not explicitly disclose a memory controller providing a non-partitioned view of said graphics memory..." However, the examiner maintains "It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a non-partitioned view of said graphics memory because the user does not need to know how the memory is partitioned." It is respectfully submitted that the examiner is citing a benefit of the current invention as a basis for rejecting the invention – this is impermissible. The examiner must identify some objective teaching in the prior art that shows or suggests the recited claim limitation. Kurihara never addresses the issue of a partitioned memory and therefore cannot be reasonably deemed to show or suggest the claimed invention.

Furthermore Kurihara does not show or suggest additional limitations associated with independent claim 32. For example, independent claim 32 is limited to a memory controller that divides "said graphics memory access bus into individual bus partitions, each of which is a

fraction of the graphics memory access bus size..." Kurihara does not show or suggest such a structure. The examiner has failed to identify any prior art that shows or suggests such a structure.

Independent claim 32 is further limited to a memory controller that partitions "information within said graphics memory into independently accessible memory partitions, said memory controller routing data from said independently accessible memory partitions to said plurality of graphics processing units via said individual bus partitions." A system that routes data from independently accessible memory partitions to individual bus partitions, as claimed, is not shown or suggested by Kurihara, which never addresses the issue of partitions. The examiner has failed to address this limitation and to otherwise identify any prior art that shows or suggests such a system.

In view of the foregoing, it is respectfully submitted that independent claim 32 is in a condition for allowance. Claims 33-54 are dependent upon claim 32 and therefore should also be in a condition for allowance.

With respect to dependent claim 34, Kurihara never addresses the issue of mapping "data to said independently accessible memory partitions in an interleaved fashion to balance memory load across independently accessible memory partitions", as claimed. The portion of Kurihara cited by the examiner does not address this limitation in even a remote manner. Therefore, the rejection of claim 34 is inappropriate.

Claim 37 recites "individual queues having corresponding arbiter circuits". The examiner acknowledges that Kurihara does not teach the claimed arbiter circuits, but maintains that they would have been obvious. It is respectfully submitted that the examiner is once again impermissibly using the benefits of the current invention to establish obviousness of the invention. The examiner has not identified any teaching in Kurihara that relates to this claim limitation. That is so because nothing in Kurihara shows or suggests the use of the claimed arbiter circuits. Therefore, the rejection of claim 37 is inappropriate. Claims 40-44 are dependent upon claim 37 and therefore their rejections are inappropriate as well. Claim 41 includes a limitation relating to a "sub-set of said plurality of graphics processing units shar[ing] a command and write data path." Kurihara wholly fails to address this issue in any way. Claim 42 is limited to a system wherein "each graphics processing unit of said sub-set of said plurality of graphics processing units has a sub-request ID." In rejecting this claim, the examiner once

again acknowledges that Kurihara does not teach this limitation, but maintains that the feature is obvious. The obviousness argument is not supported by any objective prior art teaching. Rather, once again, the examiner is relying upon the benefits of the present invention to impermissibly present an obviousness argument. Similarly, claims 43-44 include detailed limitations that are not addressed in Kurihara. The generic citation to the summary of the invention in Kurihara in no way establishes a reasonable basis for rejecting these claims.

Claims 45-49 also have detailed limitations that are not addressed in Kurihara. For each of these claims, the examiner merely cites the summary of the invention in Kurihara. The summary of the invention does not remotely relate to the limitations of these dependent claims. Therefore, the rejection of the claims is inappropriate.

Claims 50-54 relate to priority policies used by the arbiter circuits. As discussed above, Kurihara does not even show or suggest arbiter circuits. Therefore, it is especially inappropriate to maintain that Kurihara shows or suggests priority policies that may be used in connection with non-existent arbiter circuits.

Claims 55-67 include limitations of the type discussed above. Therefore, these claims should also be in a condition for allowance.

In sum, claims 32-67 have been drafted to fully distinguish over the prior art of record. Kurihara does not show or suggest the limitations of claims 32-67. Accordingly, all of the pending claims should be in a condition for allowance. If the examiner believes that any of the claims are not in a condition for allowance, he is encouraged to contact the undersigned to resolve any outstanding issues.

Dated: Aug. 20 2003

Respectfully submitted,
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